National Semiconductor

February 2004

LM4918 Boomer® Audio Power Amplifier Series
Stereo Audio Amp with AGC Control

General Description

The LM4918 is a monolithic integrated circuit that provides a automatic gain control (AGC), and stereo bridged audio power amplifiers capable of producing 1W into 8Ω with less than 1.0% THD.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4918 incorporates a AGC and stereo bridged audio power amplifiers making it optimally suited for multimedia monitors, portable radios, desktop and portable computer applications.

The LM4918 features an externally controlled, low-power consumption shutdown mode, and a power amplifier mute for maximum system flexibility and performance.

Key Specifications

- THD+N at 1kHz, 1W, 8Ω 0.3% (typ)
- Total quiescent power supply current 18mA (typ)
- Total shutdown power supply current 1µA (typ)

Features

- 0.75dB per step/32step AGC Control Interface
- Automatic Gain Control Circuitry
- Stereo Bridged power amplifiers
- “Click and pop” suppression circuitry
- Thermal shutdown protection circuitry
- Selectable Auto Detect Std-by mode and Logic control

Applications

- Portable Computers
- Desktop Computers
- Multimedia monitors

Typical Application

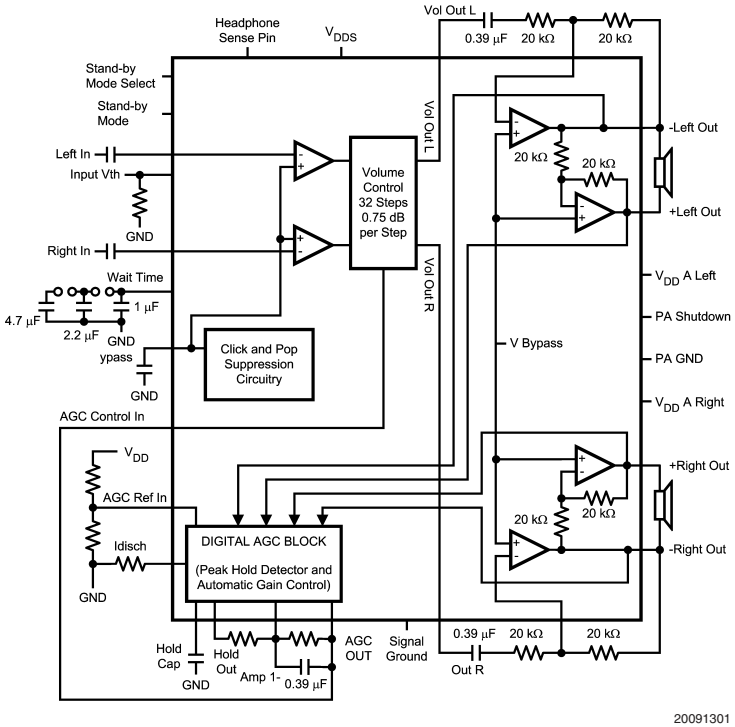

FIGURE 1. Typical Audio Amplifier Application Circuit

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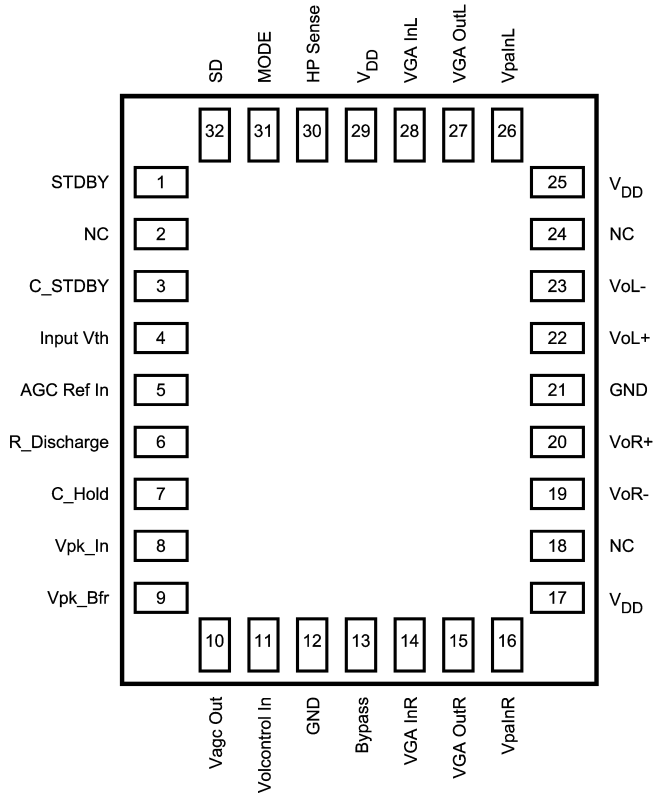
Connection Diagrams

LQ Package



20091302

Top View
Order Number LM4918LQ
See NS Package Number LQA32B

LQ Marking

200913H7

Top View
NS - Std NS Logo
U - Wafer Fab Code
Z - Assembly Plant Code
XY - 2 Digit Date Code
TT - Die Run Traceability
L4918LQ - LM4918LQ

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JA} (LLP)	51˚C/W

See AN-1187 'Leadless Leadframe Packaging (LLP).'

Operating Ratings

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-40˚C \leq T_A \leq +85˚C$
Supply Voltage	$2.7V \leq V_{DD} \leq 5.5V$

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed to T_j = 25˚C, V_{DD} = 5.0V.

Symbol	Parameter	Conditions	LM4918		Units (Limits)
			Typical	Limit	
Common Portion					
V_{DD}	Supply Voltage			2.7 5.5	V(min) V(max)
I_{DD}	Quiescent Supply Current	V_{in} = 0V, I_o = 0A	18	25	mA (max)
I_{SDIH}	Shutdown Current	$V_{SD} = V_{DD}$	1	2	µA (max)
$I_{std\text{-}by}$	Stand-By Current	$V_{std\text{-}by} = V_{dd}$	1	2	mA (max)
V_{ih}	Logic High			0.8xVdd	V (min)
V_{il}	Logic Low			0.2xVdd	V (max)
AGC Volume					
AGC Vol max	Max gain	Vol control in ≧ 4.5V	0 0	0.5 -0.5	db(max) dB(min)
AGC Vol min	Min gain	Vol control in ≦ 0.5V	-24	-22 -26	dB(max) dB(min)
AGC Step Size			.75		dB
AGC Control Block					
Vdisch	Voltage on Rdisch		1.2		V
Idisch	Discharge Current on Chold		320		nA
Vos	Offset Voltage	V_{IN} = 0V	10		mV
Av Inv	Inverting amp gain	Vagcref = 4.5V	0	±0.5	dB
Std-by Detect					
Vin	Input Sig Threshold Level		14 50		mVpk mVpk
Twait	Wait time	$C_{\_STBY}$ = 10µF	10		sec
Power Amp Block					
Vos	Output Offset Voltage	Vin = 0V	10	40	mV(max)
Po	Output Power	THD = 1%, F = 1kHz, R_l = 8Ω	1.1	1.0	W(min)
THD+N	Total Harmonic Distortion+Noise	20Hz ≦ f ≧ 20kHz, Avd = 2, R_l = 8Ω, Po = 1W	0.3		%
PSRR	Power Supply Rejection Ratio	Vdd = 5V, Vripple = 200mVrms, Rl = 8Ω, Cb = 1.0µF	67		dB
Xtalk	Channel Separation in SE	F = 1kHz, Cb = 1.0µF	60		dB
Xtalk	Channel Separation in BTL	F = 1kHz, Cb = 1.0µF	76		dB
SNR	Signal to Noise Ratio	Vdd = 5V, Po= 1.1W, R_l = 8Ω	109		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4918, see power derating curves for additional information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: R_{OUT} is measured from the output pin to ground. This value represents the parallel combination of the 10kΩ output resistors and the two 20kΩ resistors.

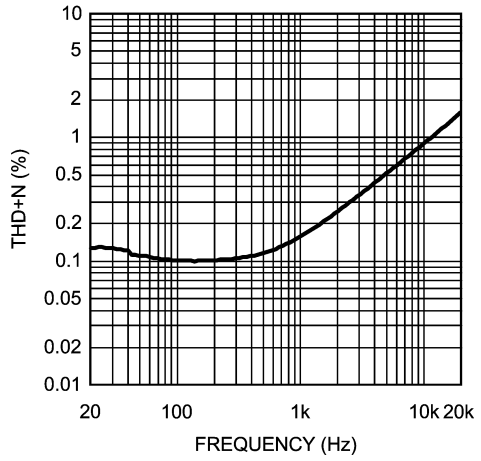
Note 10: If the product is in Shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the device will be protected. If the device is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operation life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

Note 11: Maximum power dissipation in the device (P_{DMAX}) occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 1 shown in the **Application Information** section. It may also be obtained from the power dissipation graphs.

Note 12: Data taken at VagcRef = V_{DD} and Power Amp Gain set to A = 2.

Typical Performance Characteristics (Note 12)

THD+N vs Frequency
V_{DD} = 3V, R_L = 4Ω, BTL, P_O = 225mW



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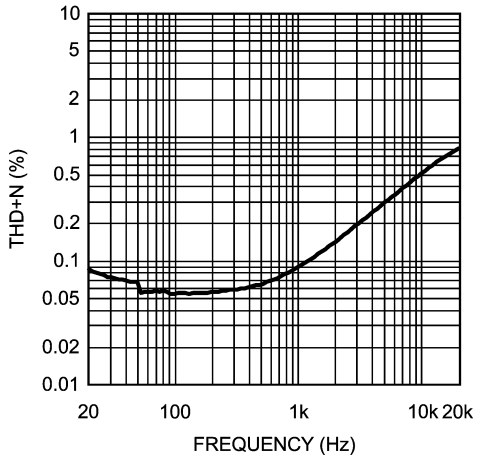
THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, BTL, P_O = 275mW



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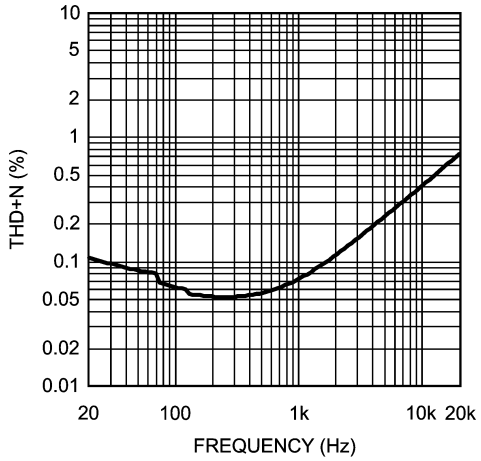
THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, BTL, P_O = 400mW



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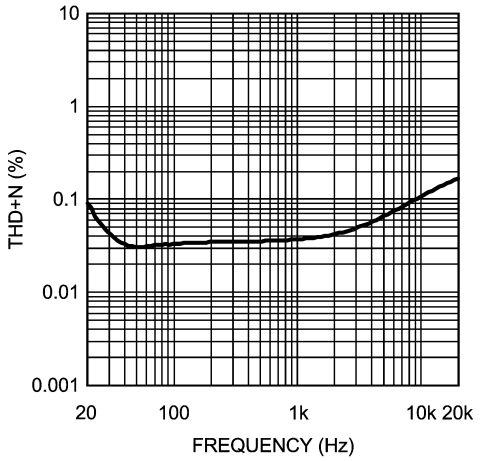
THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, SE, P_O = 40mW



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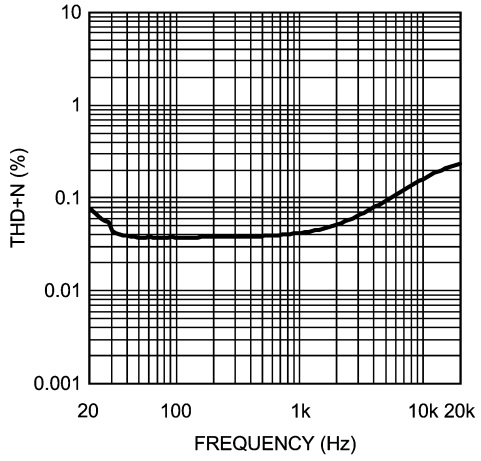
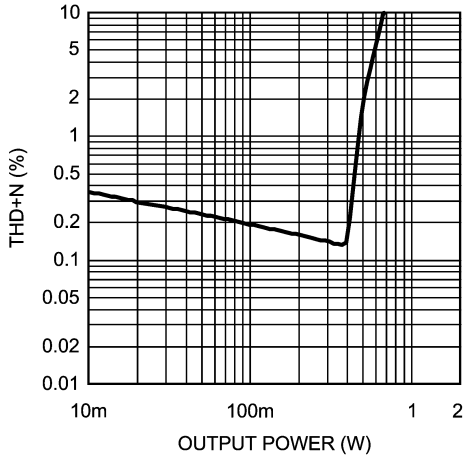
THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω, SE, P_O = 25mW



200913H5

THD+N vs Output Power
V_{DD} = 3V, R_L = 4Ω, BTL



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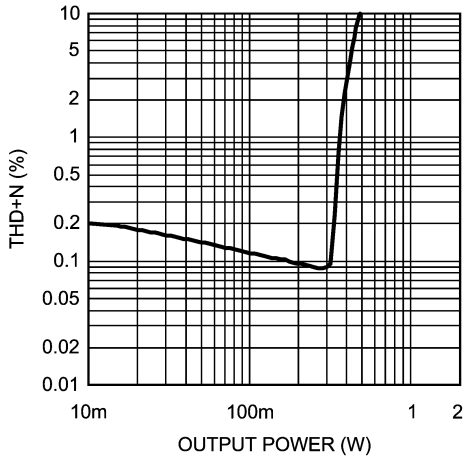
Typical Performance Characteristics (Note 12) (Continued)

THD+N vs Output Power
V_{DD} = 3V, R_L = 8Ω, BTL



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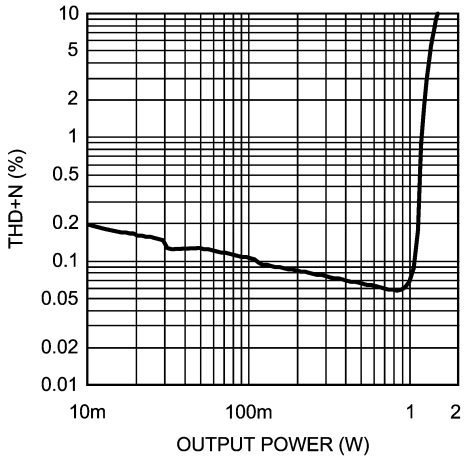
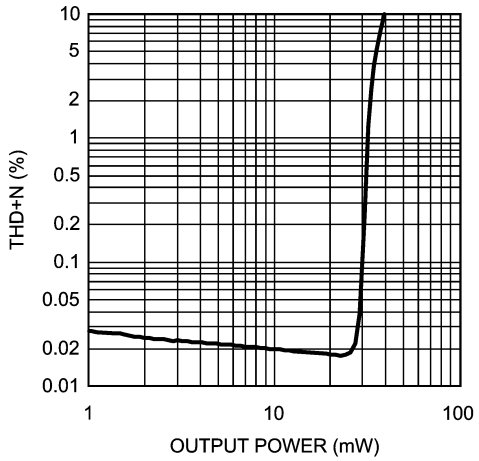
THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, BTL



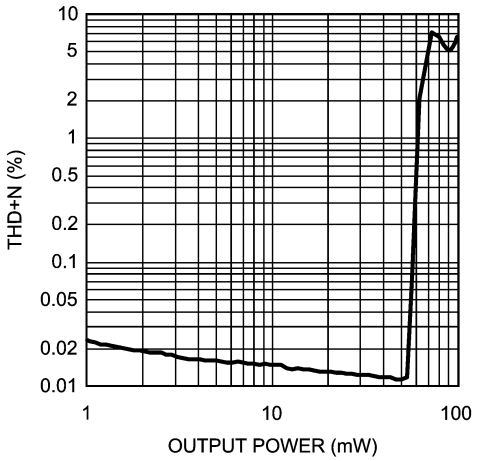
200913G1

THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω, SE



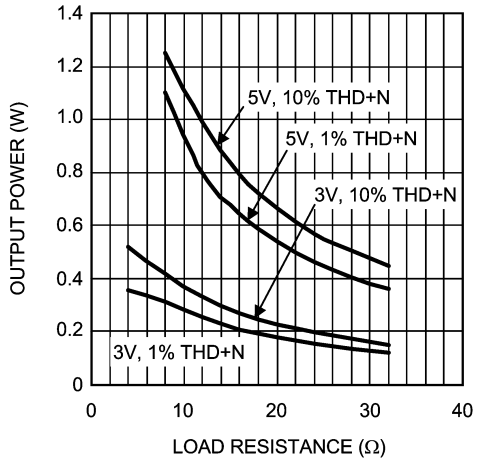
200913G2

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, SE



200913G3

Output Power vs Load Resistance
BTL



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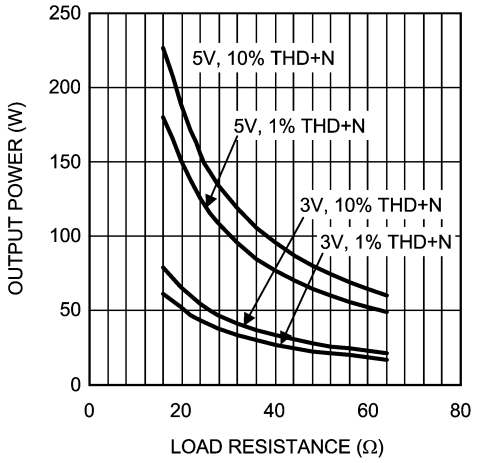
Output Power vs Load Resistance
SE



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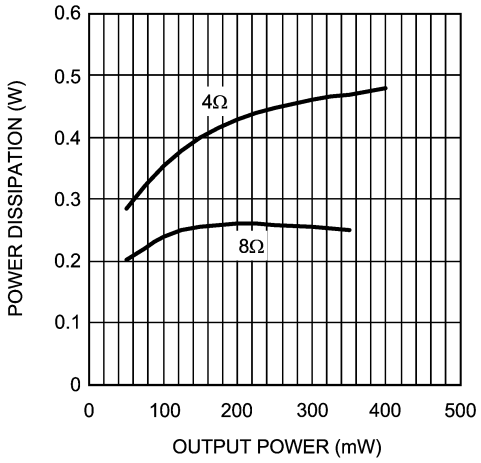
Typical Performance Characteristics (Note 12) (Continued)

Power Dissipation vs Output Power
V_{DD} = 3V, BTL



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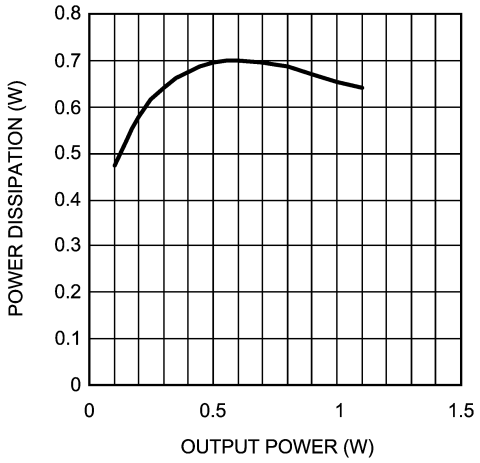
Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω, BTL



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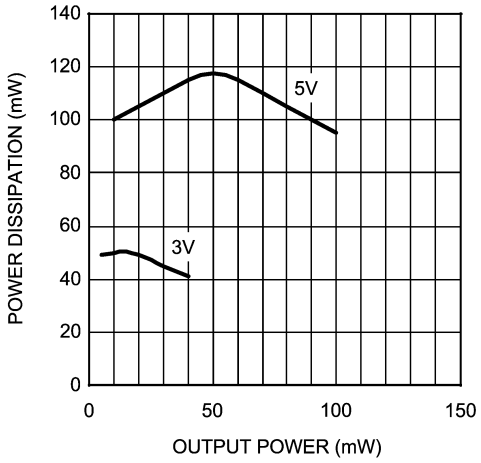
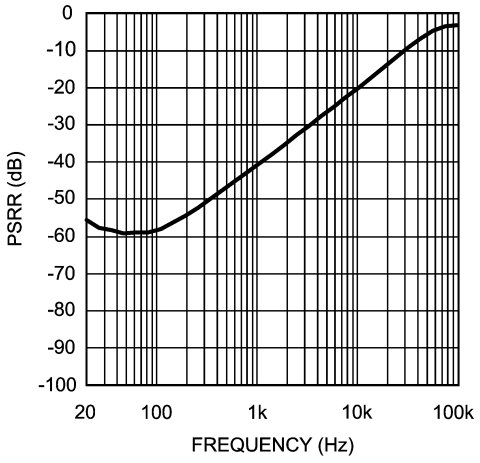
Power Dissipation vs Output Power
V_{DD} = 5V and 3V, R_L = 32Ω, SE



200913G7

PSRR vs Frequency
V_{DD} = 3V, R_L = 8Ω, BTL, Full System
Inputs 10Ω Terminated to GND



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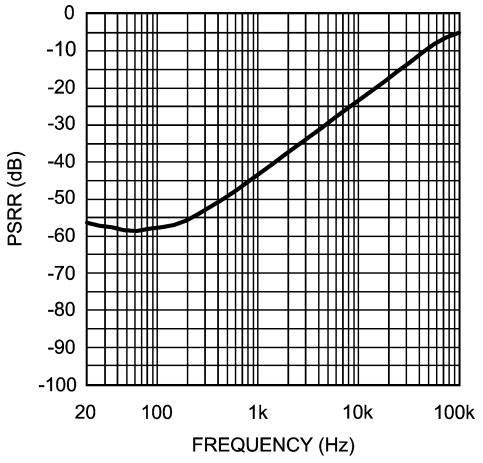
Typical Performance Characteristics (Note 12) (Continued)

PSRR vs Frequency
V_{DD} = 5V, R_L = 8Ω, BTL, Full System
Inputs 10Ω Terminated to GND



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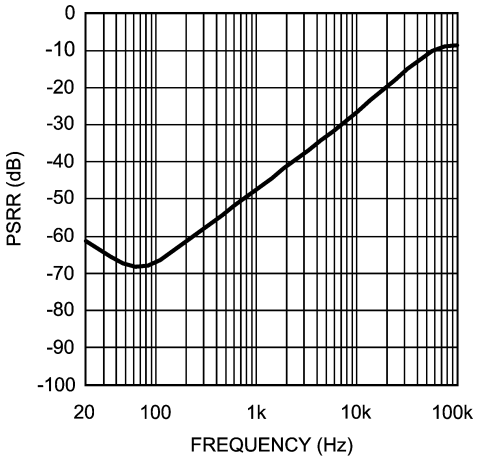
PSRR vs Frequency
V_{DD} = 3V, R_L = 32Ω, SE, Full System
Inputs 10Ω Terminated to GND



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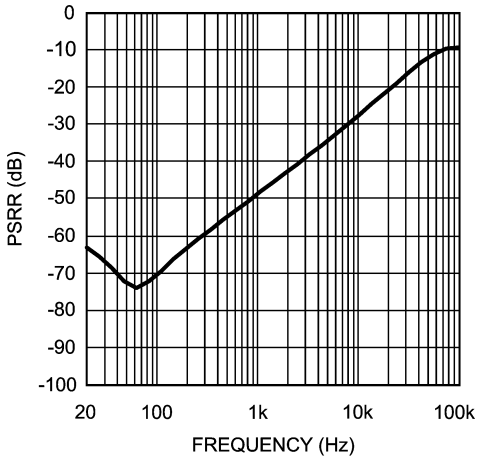
PSRR vs Frequency
V_{DD} = 5V, R_L = 32Ω, SE, Full System
Inputs 10Ω Terminated to GND



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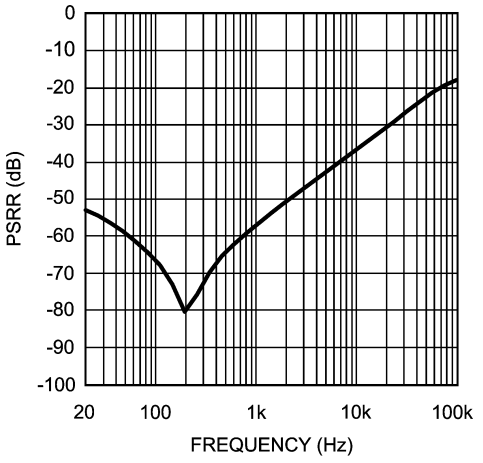
PSRR vs Frequency Power Amplifier Only
V_{DD} = 5V, R_L = 8Ω, BTL
Inputs 10Ω Terminated toGND



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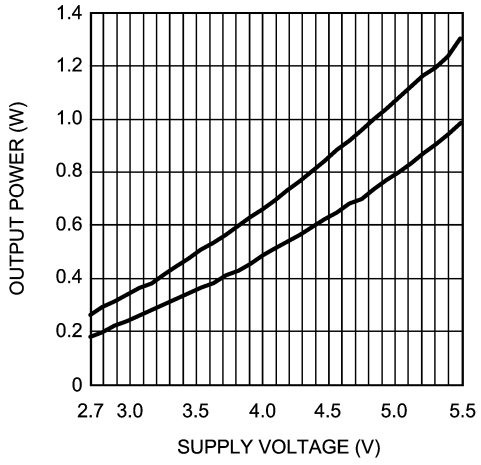
Typical Performance Characteristics (Note 12) (Continued)

Supply Voltage vs Output Power
R_L = 8Ω, BTL,10% and 1% THD+N



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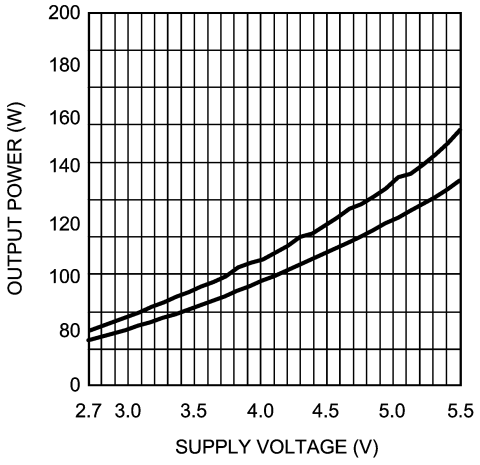
Supply Voltage vs Output Power
R_L = 32Ω, SE,10% and 1% THD+N



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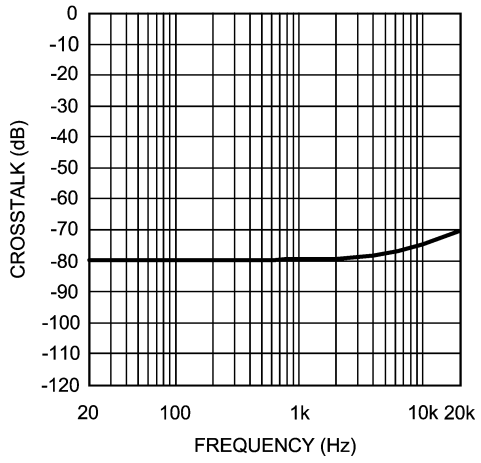
Channel Separation
V_{DD} = 5V and 3V, R_L = 8Ω, BTL



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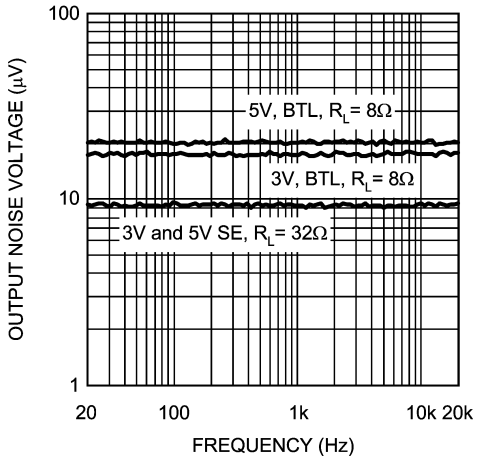
Noise Floor
A-Weighted



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Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4918 consists of two pairs of operational amplifiers, forming a two-channel (channel L and channel R) stereo amplifier. (Though the following discusses channel L, it applies equally to channel R.) External resistors Rf and Ri (set as R0 and R1, respectively for the L channel, and R7 and R6, respectively for the R channel on the demo board circuit) set the closed-loop gain of the first op-amp, whereas two internal 20kΩ resistors set the second op-amps gain at -1. The LM4918 drives a load, such as a speaker, connected between the two amplifier outputs, VoL- and VoL+ (VoR-, and VoR+ for the R channel). *Figure 1*shows that the first op-amp's output serves as the second op-amp's input. This results in both amplifiers producing signals identical in magnitude, but 180˚ out of phase. Taking advantage of this phase difference, a load is placed between VoL- and VoL+ and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 * (R_f / R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require (such as when using the LM4918 to drive single-ended headphone loads). Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4918 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (2), assuming a 5V power supply and a 8Ω load, the maximum single channel power dissipation is 0.158W or 0.317W for stereo operation.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Bridge-Mode} \quad (3)$$

The LM4918's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX'} = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

The LM4918's T_{JMAX} = 150˚C. In the LQ package soldered to a DAP pad that expands to a copper area of 1in^2 on a PCB, the LM4918's θ_{JA} is 51˚C/W. At any given ambient temperature T_A, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting P_{DMAX} for $P_{DMAX'}$ results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4918's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX}\theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 85˚C for the LQ package.

$$T_{JMAX} = P_{DMAX}\theta_{JA} + T_A \quad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the LM4918's 150˚C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4918's exposed-DAP (die attach paddle) packages (LD) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.1W dissipation in an 8Ω load at ≤ 1% THD+N. This power is achieved through careful consideration of necessary thermal design. Failing to opti-

Application Information (Continued)

mize thermal design may compromise the LM4918's performance and activate unwanted, though necessary, thermal shutdown protection.

The LM4918LD must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally, connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with 2 vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LQ (LLP) package is available in National Semiconductor's AN1187.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4918's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4918's power supply pin and ground as short as possible. Connecting a 2.2µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance system cost, and size constraints.

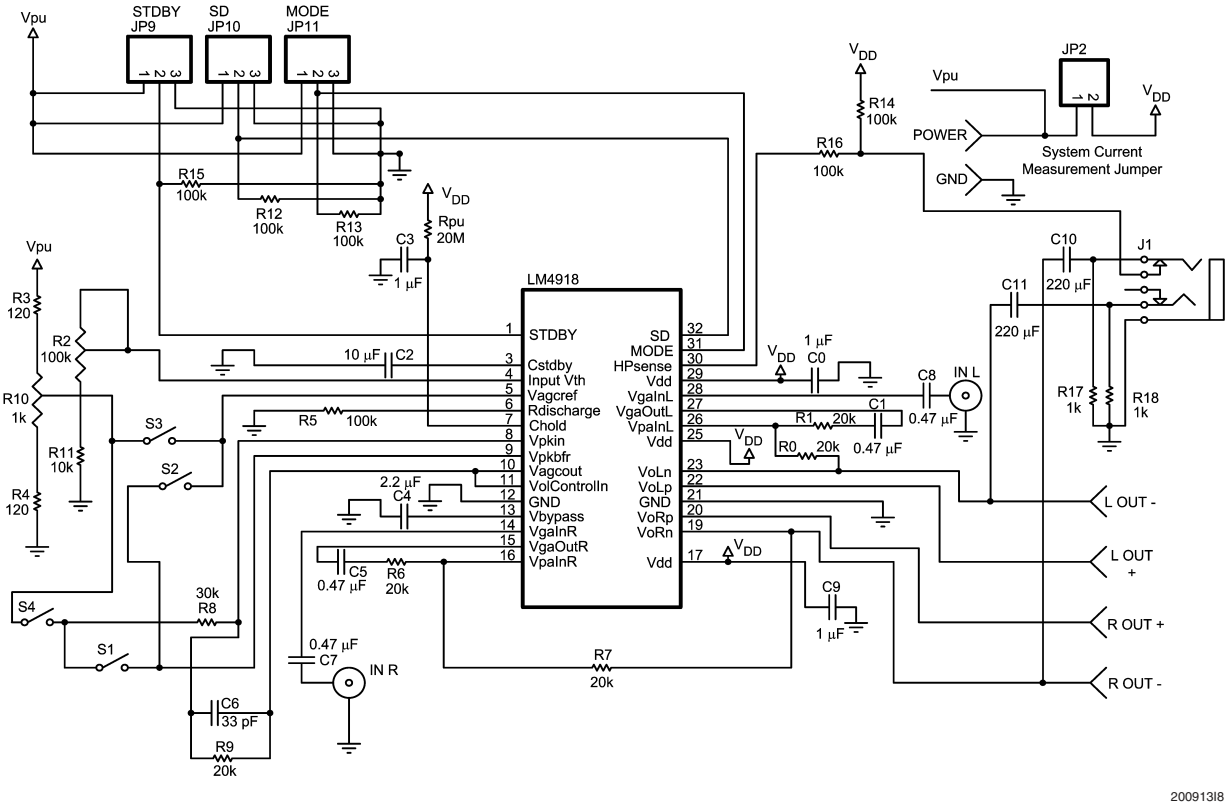


FIGURE 2. REFERENCE DESIGN BOARD SCHEMATIC

Application Information (Continued)

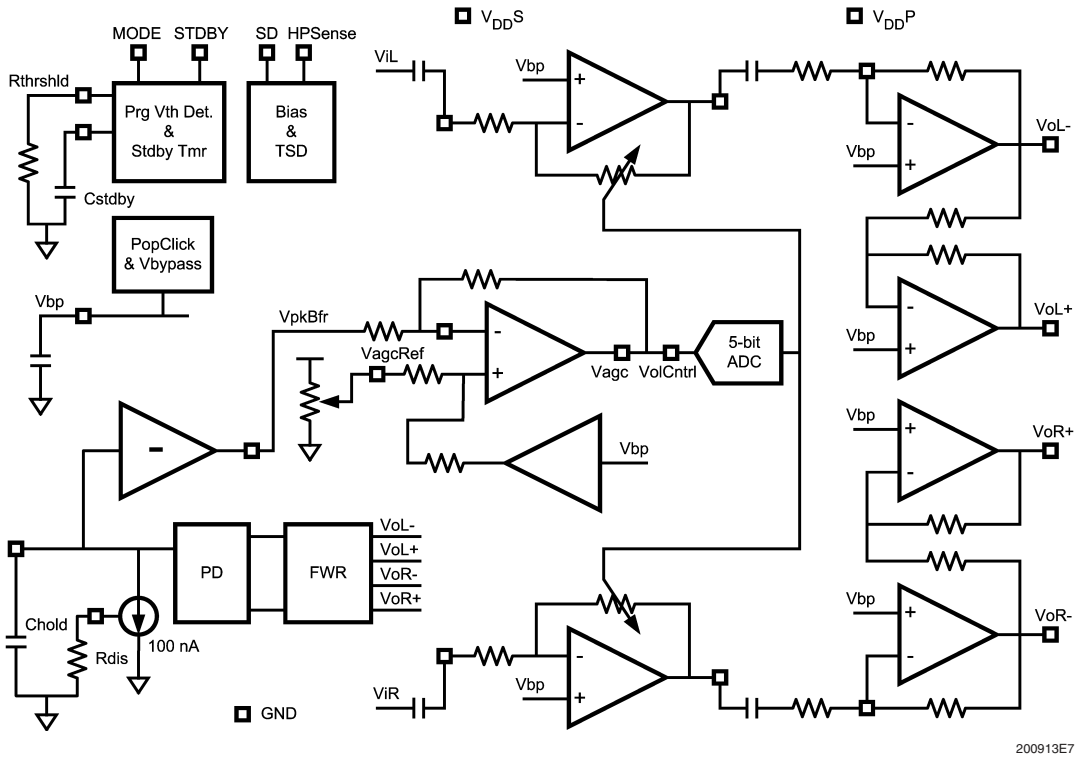


FIGURE 3. Block Diagram with external component for AGC closed loop

AUTOMATIC GAIN CONTROL (AGC)

The AGC represents a closed loop gain control network in conjunction with the peak detect monitoring the outputs of the power amplifier section. A reference voltage is put on the "AGC Ref In" pin to set the desired dynamic range of the AGC. This voltage should be set to allow for maximum desired output level for the expected range of the input signal. The AGC may provide anywhere from 0 to 24dB of attenuation. The peak detect constantly updates the AGC block with information about the maximum level of the output signal. Internally, if this peak value is higher than the set reference voltage, the AGC will reduce the gain of the circuit until the output peak is lower than the reference voltage. This entire process is timed by the Chold capacitor (in conjunction with Rdischarge), which determines the hold time between peaks while restoring gain (gain returns to normal levels after being attenuated by large power amp output signal).

The circuit shown in Figure 3 best describes the AGC loop operation. Square nodes are external pins. Vbp is the bypass voltage. As is shown below, the peak detect section (PD) monitors all outputs of the power amp (VoL+, VoL-, VoR+, and VoR-). Peaks are fed into the peak buffer, regulated by Chold and Rdis. The output of the peak buffer (VpkBfr) is then compared to VagcRef. The AGC amplifier then sets the ADC output to control the gain setting in 32 discrete steps from 0 to −24dB. Gain will remain reduced until peak levels (Vpkbfr) return below the VagcRef, as buffered by the peak buffer and Chold. This means gain will slowly increase (speed determined by Chold) back to normal levels (maximum gain set) or until the peaks again exceed the reference level.

The reference voltage VagcRef should be set in conjunction with the gain settings on the power amplifier stage to provide maximum gain (0dB) for the typical desired maximum output level of the part for a maximum input level. This will ensure that both the full 24dB dynamic range of the AGC is used effectively and that maximum effective audio levels may be reached without clipping. Typical AGC peak gain values for given VagcRef voltages are shown in Table 1. These are taken with a 20MΩ pullup resistor on Chold (as used shown on the demo board). These are shown as typical values only – VagcRef level should be set with the factors described above.

Application Information (Continued)

TABLE 1. Typical VAGCREF Values

STEP	AGC Peak Gain Level (dB)	VagcRef (V)
1	-0.1	4.1
2	-1.6	4.0
3	-2.4	3.9
4	-3.1	3.8
5	-3.8	3.7
6	-4.6	3.6
7	-5.4	3.5
8	-6.1	3.3
9	-6.9	3.2
10	-7.6	3.1
11	-8.4	3.0
12	-9.1	2.9
13	-9.8	2.7
14	-10.6	2.6
15	-11.4	2.4
16	-12.1	2.3
17	-12.8	2.1
18	-13.6	2.0
19	-14.4	1.8
20	-15.1	1.7
21	-15.9	1.6
22	-16.6	1.4
23	-17.3	1.3
24	-18.1	1.2
25	-18.8	1.1
26	-19.6	1.0
27	-20.3	0.8
28	-21.1	0.7
29	-21.8	0.5
30	-22.6	0.3
31	-23.4	0.2
32	-24.2	0

Application Information (Continued)

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4918 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic high (0.8 x V_{DD}) is placed on the shutdown pin. By switching the shutdown pin to V_{DD}, the LM4918 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than 0.8V_{DD}, the idle current may be greater than the typical value of 1µA. (Idle current is measured with the shutdown pin at V_{DD}).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-down resistor. When the switch is closed, the shutdown pin is connected to V_{DD} and disables the amplifier. If the switch is open, then the external pull-down resistor will enable the LM4918. This scheme guarantees that the shutdown pin will not float thus preventing unwanted state changes.

STANDBY

When in MODE 0, activating Standby with a logic high (0.8 x V_{DD}) maintains the outputs at their bias level, but with no signal. This allows for extremely fast (less than 1ms) turn off/on of the audio outputs with a minimum current draw while in Standby mode (1mA typ).

When in MODE 1, enabling/disabling Standby is also dependant upon the input signal level and the input threshold setting. In this mode, Standby is not enabled until both a logic high is placed on the Standby pin and the input signal level has remained below the set input threshold level for a period of time determined by Chold (typically a few seconds). This delay time set by Cstdby prevents the LM4918 from inadvertently triggering Standby mode during quiet passages in music. Returning from Standby while in MODE 0 is also dependant upon both a logic low on the Standby pin and the input signal level being above the set threshold. In this case, however, return from Standby is immediate and does not require the input to remain above the threshold level for any amount of time.

STANDBY MODE SELECT

The LM4918 has two user-selectable modes for standby usage. The first mode (MODE 0), valid when MODE is equal to logic low (0.2 x V_{DD} or less), is characterized by the immediate activation of Standby mode (outputs remain at bias point, with no signal) when a logic high is applied to the Standby pin, and the immediate return from Standby upon a logic low on the Standby pin.

The second mode (MODE 1), valid when MODE is equal to logic high (0.8 x V_{DD}), is characterized by a delayed activation of Standby mode. In this case Standby is delayed until both a logic high is placed on the Standby pin and the input signal has maintained a value below the input threshold (as determined by the resistance on Input Vth) for a given amount of time (determined by Cstdby). Returning from Standby also requires both a logic high on the Standby pin and a sufficiently large input signal to overcome the set input threshold. No hold time applies to return from Standby – deactivation is immediate upon both conditions being met.

INPUT THRESHOLD DETECT

The LM4819 has an input threshold detect function that works in conjunction with the Standby mode and is only enabled when the LM4918 is in MODE 1 (see STANDBY MODE SELECT). This threshold level may be set anywhere from 14mV to 50mV (typical peak values) by adjusting the resistance placed from Input Vth to GND. Typical values have about 50kΩ for a 14mVpk level and 15kΩ for a 50mVpk level. Care should be taken not to set the threshold values too low, as the part may cycle in and out of shutdown if any spurious noise was present on the inputs. For this reason, threshold values less than 14mVpk with corresponding resistance values greater than 50kΩ are not recommended.

This threshold value sets the peak input level that must be exceeded for the part to return from Standby when in MODE 1. It also is the level which the input must remain below (for an amount of time determined by Cstdby) for the part to enter Standby when in MODE 1.

HP SENSE FUNCTION

Applying a voltage greater than 0.8V_{DD} to the LM4918's HP Sense pin turns off the second amplifier on each channel, muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 2 shows the implementation of the LM4918's headphone sense function. With no headphones connected to the headphone jack, the R14-R17 voltage divider sets the voltage applied to the HP Sense pin (pin 30) at approximately 50mV. This 50mV enables the second amplifiers, placing the LM4918 in bridged mode operation. The output coupling capacitor blocks the amplifier's half supply DC voltage, protecting the headphones.

The HP Sense threshold is set at 0.8V_{DD}. While the LM4918 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from VoR– and allows R14 to pull the HP Sense pin up to V_{DD}. This enables the headphone function, turns off the second amplifiers, and mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistor R17 and R18. These resistors have negligible effect on the LM4918's output drive capability since the typical impedance of headphones is 32Ω.

Figure 2 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP Sense pin when connecting headphones. A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP-IN pin, a bridge-connected speaker is muted and the first set of amplifiers drive a pair of headphones.

PEAK DETECT

The LM4918 also incorporates a peak-detect function to properly monitor output level in conjunction with the AGC. This peak detect function may be set for positive or negative detect, based on the users preference. On the demo board, shown in Figure 2, both circuits are available for testing. The normal, positive peak detect, is engaged by inserting jumpers at S1 and S3, while removing jumpers at S2 and S4. The

Application Information (Continued)

negative peak circuit is described by jumpers in place on S2 and S4, while removed from S1 and S3. Operating in the negative manner places the Vpk_Bfr directly to VagcRef, and makes Vpk_in the effective AGC gain reference voltage. Keep in mind this will reverse the voltage values used for a given AGC gain level as compared to VagcRef values.

The peak detect period is set by the Chold capacitor as described in the **AUTOMATIC GAIN CONTROL** section. AGC gain will slowly increase to maximum set value at a rate determined by Chold. Decreasing Chold results in faster peak hold times and faster gain increase after a peak-induced gain reduction.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C7 and C8 in Figure 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The LM4918 actually has two different sets of input coupling caps: one for the AGC block (C7 and C8) and one for the power amplifier block (C1 and C5). These must both be in place to properly protect the inputs from DC offsets and should match for predictable frequency response.

The internal input resistor (R1 and R6) and the input capacitor (C1 and C5) produce a high pass filter cutoff frequency that is found using Equation (7).

$$f_c = 1 / (2\pi RC) \quad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation (7) is 0.063µF. The 0.49µF C_i shown in Figure 2 allows the LM4918 to drive high efficiency, full range speaker whose response extends below 20Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the Vbypass pin. Since C_B determines how fast the LM4918 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4918's outputs ramp to their quiescent DC voltage (nominally V_{DD}/2), the smaller the turn-on pop. Choosing C_B equal to 2.2µF along with a small value of C_i (in the range of 0.1µF to 0.49µF), produces a click-less and pop-less shutdown function.

Output Capacitor Value Selection

Amplifying the lowest audio frequencies also requires the use of a high value output coupling capacitor (C10 and C11 in Figure 2). A high value output capacitor can be expensive and may compromise space efficiency in portable design. The speaker load (R) and the output capacitor (C) form a high pass filter with a low cutoff frequency determined using Equation (7).

When using a typical headphone load of $R_L = 32\Omega$ with a low frequency limit of 50Hz, C_O is 99µF. The 200µF C_O shown in Figure 2 allows the LM4857 to drive a headphone whose frequency response extends below 50Hz.

Cstdby Value Selection

Cstdby is set to provide a large enough delay time on the threshold detect such that the device does not inadvertently toggle in and out of Standby mode when in MODE 1 and low level music passages are playing. This should be set for delay periods of several seconds. The demo board uses a 10uF cap that results in about 10s (typ) of delay time before entering Standby (MODE 1 must be enabled, Standby must be enabled, and the input level must remain below the threshold level for 10s). Smaller values may result in Standby activation during extended low periods of music.

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATION

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signal traces should be located as far away as possible from analog components and circuit traces.

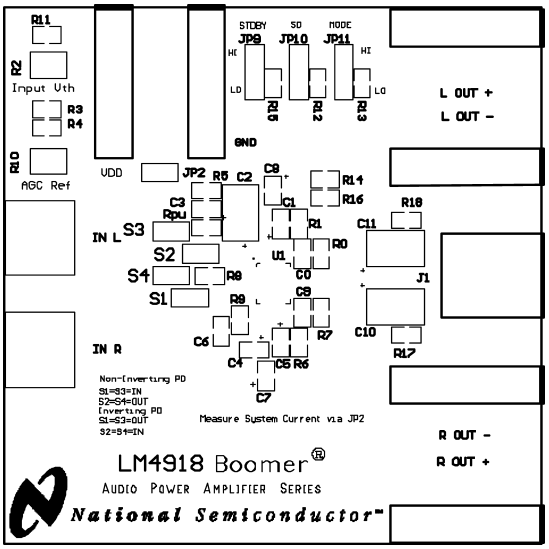
Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Application Information (Continued)

LM4918 LLP BOARD ARTWORK

Top Overlay



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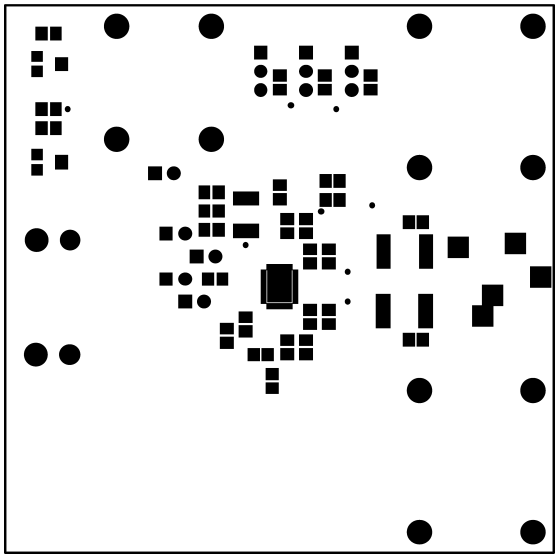
Top Solder



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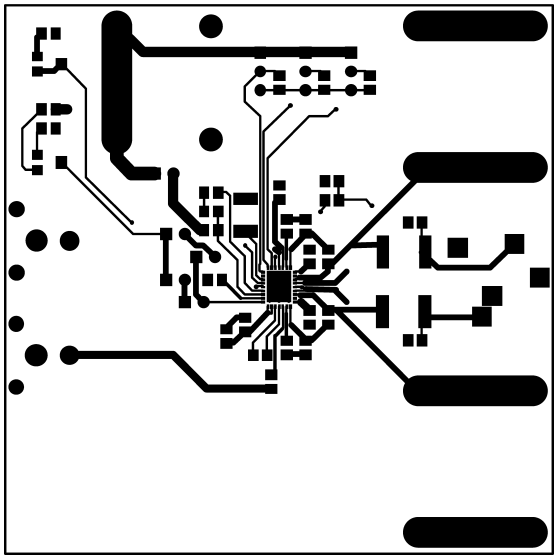
Top Layer



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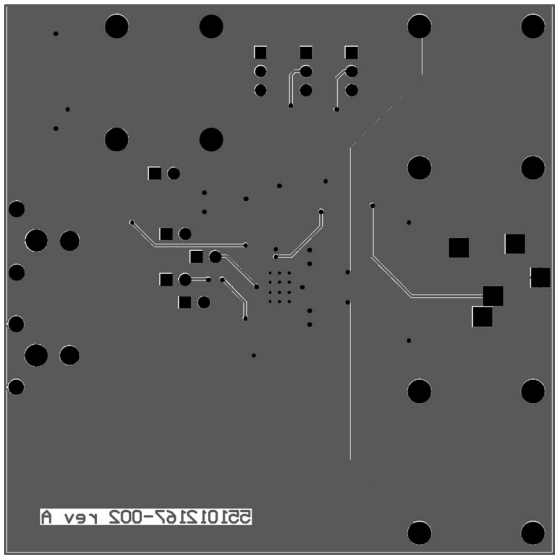
Bottom Layer



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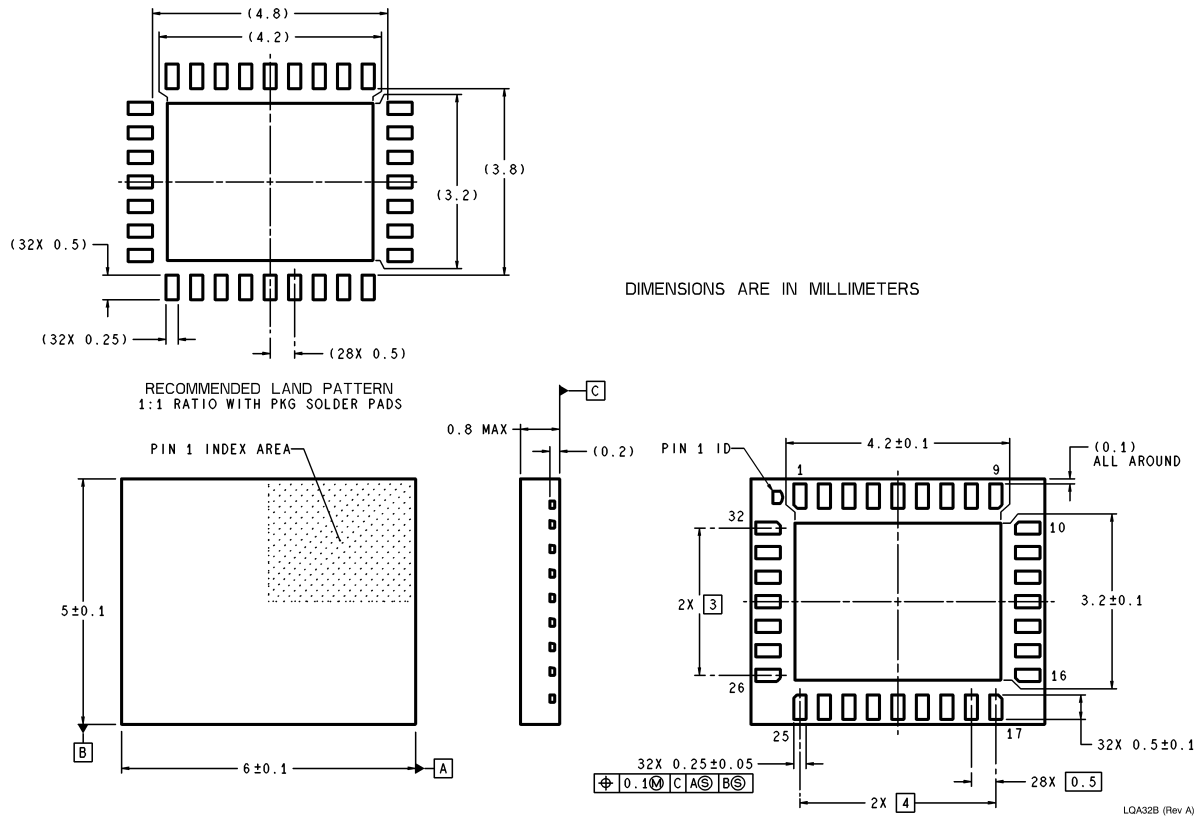
Physical Dimensions inches (millimeters) unless otherwise noted



LQ Package
Order Number LM4918LQ
NS Package Number LQA32B

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